SOLUTION – CS 250 Fall 2017 Homework 02

Due 11:58pm Thursday, Sept. 07, 2016

\*\*\* Submit your solution via Blackboard in PDF file format.

1. A logic gate of a new technology recognizes voltages in the range from 0.0 V to +0.9 V as logic 0 and voltages in the range from Vdd to Vdd – 1.2 V as logic 1. Vdd  stands for a variable supply voltage amount, because this logic gate is designed to reduce its power consumption by accepting reduced supply voltage with a trade-off that the gates will switch less quickly (slower performance but lower power). Use of this capability could be commanded by the operating system when the computer workload is known to be low. When the workload increases, then the supply voltage could be increased.  
   Assume that Vdd =5 V is the supply voltage used for the highest workload. In addition to 5 V which of the following are plausible Vdd values and why: 4 V, 3 V, and 2 volts?

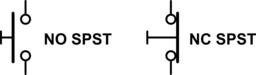
The Vdd voltage of 2v would not work. The reason is that we are given that a voltage of between Vdd and Vdd - 1.2v will be recognized as a logic 1. That means that a voltage as low as 0.8v would be considered a logic 1.

However, we are also given that a voltage of between 0 and 0.9v would be considered a logic 0. This sets up a conflict where any voltage between 0.8 and 0.9v would be both a logic 0 and a logic 1, causing the circuit to fail.

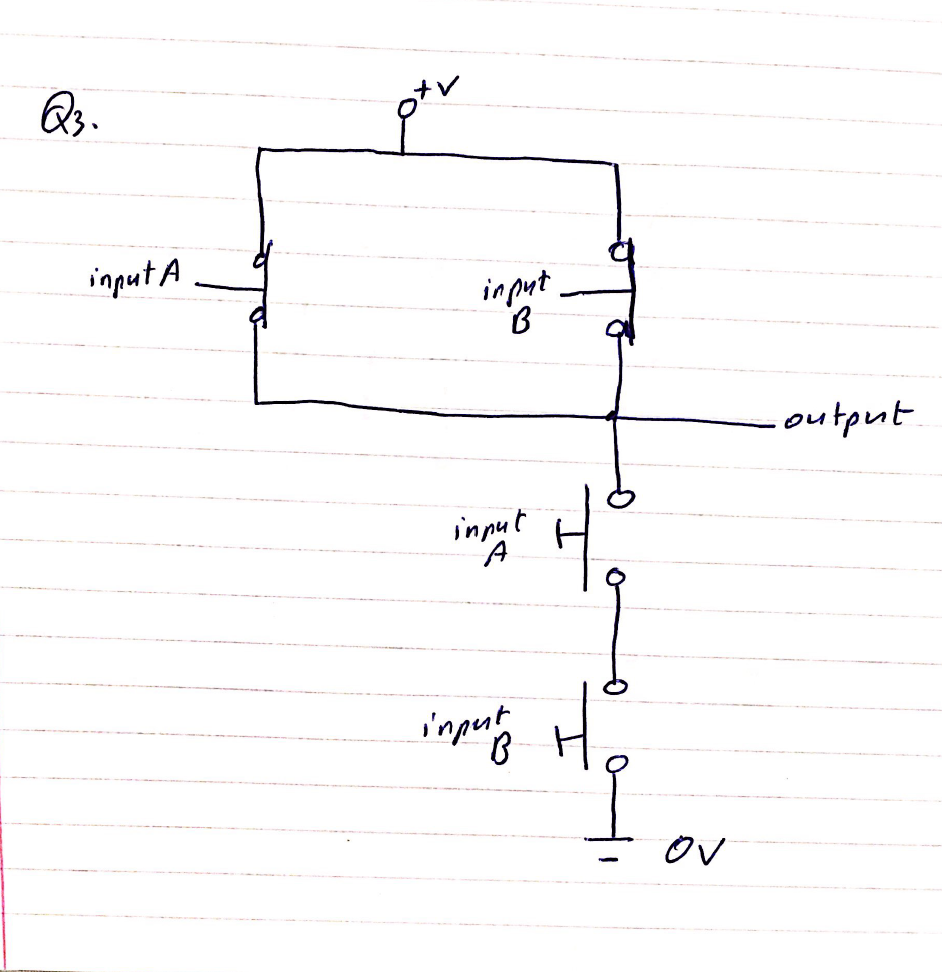
The Vdd voltages of 3v and 4v avoid this conflict and would work.

1. If it is it true that X⊙X’ = 1, then what Boolean algebra operation is being represented by the ⊙ symbol?

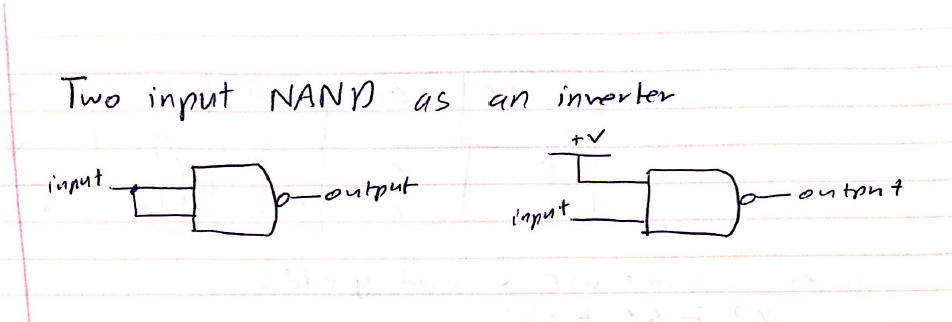
If X is 0 then X' is 1 , now X OR X' is 1  
If X is 1 then X' is 0 , now X OR X' is 1  
Hence the symbol given is OR.

1. The normally-open (NO) single-pole, single-throw (SPST) push button switch (same type as in the lab kit) transitions from high resistance to low resistance when pushed. A normally-closed (NC) SPST push button switch reverses this behavior. The schematic symbols for these two switches are shown here.   
   

Using only switches of these two types, wire, and connections to +5 V and ground, draw a schematic to implement (AB)’. Clearly label your inputs and output.

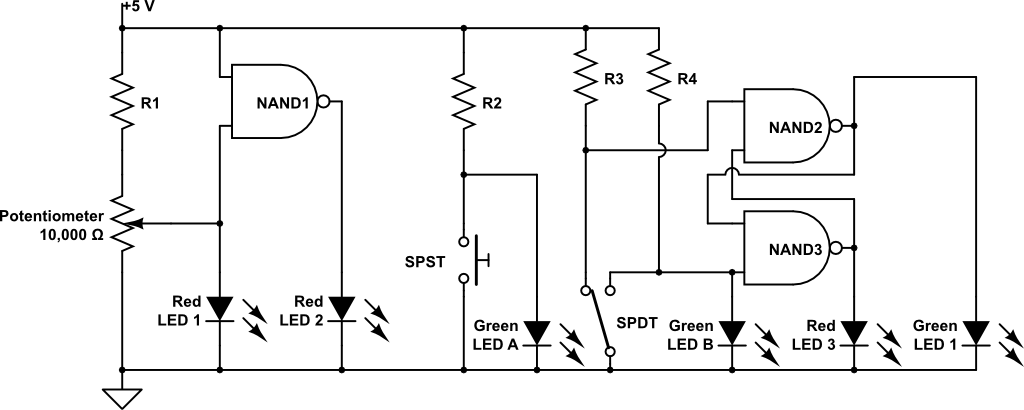


1. Draw a schematic showing two ways to use a two-input NAND as an inverter.



1. If propagation delay in a combinatorial circuit is measured in units of gate delays, how long before all outputs are valid for an 8-bit ripple carry adder circuit?

The first gate has three delays then every other one after that has 2 since the first gate has been processed in them so 7\*2 = 14 +3 = 17

1. Consider the schematic below for the following questions.  
     
   1. Green LED A will light when the SPST switch is pushed/not pushed?

Will light when not pushed

* 1. The SPDT switch pole is being moved back and forth between the contact associated with R3 and the contact associated with R4. By design, there is always a time when the moving switch pole is in contact with neither R3 nor R4. In terms of the SPDT switch positions, carefully describe when Red LED3 will light.

When the switch is not connected the current flowing through that positon is 0.   
When SPDT is connected to any position it is represented by 1. When SPDT is not connected to any position it is represented by 0. Considering the SPDT left position is 1 and right position is 2. When SPDT is not connected to either of those positions NAND 2 gets input 1 and 1and output from NAND 2 is 0. NAND 3 gets input 0 and 1 and the output is 1 and so LED 3 glows. When SPDT is connected to position 2 NAND 2 gets input 1 and 1 and the output is 0. NAND 3 gets input 0 and 0 and the output is 1 and LED 3 will glow.